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UNITED STATES PATENT APPLICATION

OF

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FOR

GaAs/Al(Ga)As DISTRIBUTED BRAGG REFLECTOR ON InP

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BACKGROUND OF THE INVENTION

Field of the Invention

[001] This invention relates to vertical cavity surface emitting lasers. More specifically, it relates to GaAs/Al(Ga)As Distributed Bragg Refelectors (DBRs) as used in vertical cavity surface emitting lasers.

Discussion of the Related Art

[002] Vertical cavity surface emitting lasers (VCSELs) represent a relatively new class of semiconductor lasers. While there are many variations of VCSELs, one common characteristic is that they emit light perpendicular to a wafer's surface. Advantageously, VCSELs can be formed from a wide range of material systems to produce specific characteristics.

[003] VCSELs include semiconductor active regions, which can be fabricated from a wide range of material systems, distributed Bragg reflector (DBR) mirrors, current confinement structures, substrates, and contacts. Because of their complicated structure, and because of their material requirements, VCSELs are usually grown using metal-organic chemical vapor deposition (MOCVD).

[004] Figure 1 illustrates a typical VCSEL 10. As shown, an n-doped gallium arsenide (GaAs) substrate 12 has an n-type electrical contact 14. An n-doped lower mirror stack 16 (a DBR) is on the GaAS substrate 12, and an n-type graded-index lower spacer 18 is disposed over the lower mirror stack 16. An active region 20, usually having a number of quantum wells, is formed over the lower spacer 18. A p-

type graded-index top spacer 22 is disposed over the active region 20, and a p-type top mirror stack 24 (another DBR) is disposed over the top spacer 22. Over the top mirror stack 24 is a p-type conduction layer 9, a p-type cap layer 8, and a p-type electrical contact 26.

[005] Still referring to Figure 1, the lower spacer 18 and the top spacer 22 separate the lower mirror stack 16 from the top mirror stack 24 such that an optical cavity is formed. As the optical cavity is resonant at specific wavelengths, the mirror separation is controlled to resonant at a predetermined wavelength (or at a multiple thereof). At least part of the top mirror stack 24 includes an insulating region 40 that provides current confinement. The insulating region 40 is usually formed either by implanting protons into the top mirror stack 24 or by forming an oxide layer. In any event, the insulating region 40 defines a conductive annular central opening 42 that forms an electrically conductive path though the insulating region 40.

[006] In operation, an external bias causes an electrical current 21 to flow from the p-type electrical contact 26 toward the n-type electrical contact 14. The insulating region 40 and the conductive central opening 42 confine the current 21 such that the current flows through the conductive central opening 42 and into the active region 20. Some of the electrons in the current 21 are converted into photons in the active region 20. Those photons bounce back and forth (resonate) between the lower mirror stack 16 and the top mirror stack 24. While the lower mirror stack 16 and the top mirror stack 24 are very good reflectors, some of the photons leak out as light 23 that travels along an optical path. Still referring to Figure 1, the light 23 passes through the p-type conduction layer 9, through the p-type cap layer 8, through

an aperture 30 in the p-type electrical contact 26, and out of the surface of the vertical cavity surface emitting laser 10.

[007] It should be understood that Figure 1 illustrates a typical VCSEL, and that numerous variations are possible. For example, the dopings can be changed (say, by providing a p-type substrate), different material systems can be used, operational details can be tuned for maximum performance, and additional structures, such as tunnel junctions, can be added. Furthermore, with long wavelengths it is often beneficial to insert a reversed biased n++/p++ tunnel junction between the top spacer 22 and the active region 20, and to change the doping type of the top structures to n-type. This is because p-doped materials absorb more light than n-doped materials, and with longer wavelengths the optical gain become more critical. The tunnel junction converts electrons into holes, which are then injected into the active region.

[008] While generally successful, VCSELs have problems. For example, a major problem in realizing commercial quality long wavelength VCSELs is the available mirror materials. Long wavelength VCSELs are often based on InP material systems. For proper lattice matching, an InP-based VCSEL usually uses InP/InGaAsP or AlInAs/AlInGaAs mirrors. However, because those materials have relatively low refractive index contrasts, 40-50 mirror pairs are typically needed to achieve the required high reflectivity. Growing that number of mirror pairs takes a long time, which increases the production costs.

[009] Other mirror material systems have been tried. For example, "Metamorphic DBR and tunnel-Junction Injection: A CW RT Monolithic Long-Wavelength VCSEL," IEEE Journal of Selected topics In Quantum Electronics, vol.

5, no. 3, May/June 1999, describes an InP-InGaAsP DBR, a GaAlAsSb-AlAsSb DBR, and a GaAlIsSb-AlAsSb DBR. Furthermore, that article describes using a reversed biased n++/p++ tunnel junction for injecting current into the active layer. While such mirror material systems are advantageous, their lattice match, refractive index contrast, and thermal conductivity characteristics are not optimal. Additionally, GaAs/Al(Ga)As is still considered to form the best distributed Bragg reflector mirrors because of its high refractive index contrast, high thermal conductivity, and the feasibility of using oxidation to enable the formation of oxide insulating regions 40.

[0010] Thus, new long wavelength VCSELS would be beneficial. Also beneficial would be GaAs/Al(Ga)As top DBRs that are fabricated on InP. Also beneficial would be a method of fabricating GaAs/Al(Ga)As top DBRs in InP-based VCSELs. Furthermore, a new type of InP based VCSEL having GaAs/Al(Ga)As top DBRs and bottom mirror systems comprised of different materials also would be beneficial.

SUMMARY OF THE INVENTION

[0011] Accordingly, the principles of the present invention are directed to VCSEL device structures suitable for use in long wavelength VCSELS. Those principles specifically provide for a new method of growing GaAs/Al(Ga)As top DBRs on InP materials. Those principles further provide for InP-based VCSELS having GaAs/Al(Ga)As top DBRs. Such VCSELS can be fabricated with bottom mirrors comprised of different material systems. Therefore, the principles of the present invention directly provide for VCSELS device structures that enable InP-

based VCSELs having GaAs/Al(Ga)As top mirror DBRs and bottom mirror systems of different materials.

[0012] A GaAs/Al(Ga)As top DBR according to the principles of the present invention is grown on InP using MOCVD and multi-step processing. The multi-step processing proceeds as follows. First, an InP layer (such as an InP spacer or an InP-based active layer) is formed. Then, an MOCVD growth temperature is set to about 400-450 °C. Then, a 20-40 nanometer thick, fast GaAs layer is grown on the InP layer. After that, the temperature is increased to around 600 °C. A high temperature GaAs seed layer, about 100 nm thick, is then grown on the low temperature GaAs layer. Beneficially, an insulation layer comprised of SiO_2 or Si_2N_4 is formed on the GaAs seed layer. If used, that insulation layer is patterned to form an opening. Then, a high temperature GaAs/Al(Ga)As top DBR is grown on the GaAs seed layer. The GaAs/Al(Ga)As mirror is beneficially grown using lateral epitaxial overgrowth.

[0013] A VCSEL according to the principles of the present invention includes a bottom DBR mirror on an InP substrate, which is beneficially n-doped. Then, an n-doped bottom InP spacer is grown on the bottom DBR mirror. Beneficially, an active region having a plurality of quantum wells is then grown on the n-doped InP spacer. Beneficially, a reversed biased tunnel junction is disposed over the active region. An n-doped top InP spacer is then beneficially grown on the tunnel junction. Also beneficially, an n-doped GaAs/Al(Ga)As top DBR is grown on the n-doped top InP spacer.

[0014] Preferably, the GaAs/Al(Ga)As top DBR is grown by a multi-step process using MOCVD. First, the growth temperature is set to 400-450 °C. Then, a

20-40 nanometer thick low temperature GaAs layer is grown on the n-doped top InP spacer. After that, the temperature is increased to around 600 °C. A high temperature GaAs seed layer, about 100 nm thick, is then grown on the low temperature GaAs layer. Then an insulation layer comprised of SiO_2 or Si_2N_4 is formed on the GaAs seed layer. The insulation layer is patterned to form an opening. A high temperature GaAs layer is then grown on the GaAs seed layer, followed by a GaAs/Al(Ga)As top DBR. The high temperature GaAs layer and the GaAs/Al(Ga)As mirror are beneficially grown using lateral epitaxial overgrowth.

[0015] Beneficially, a VCSEL according to the principles of the present invention includes a bottom DBR fabricated using a material system that is compatible with InP. For example, the bottom mirror could be an AlPSb/GaPsb DBR mirror, an AlGaInAs/AlInAs DBR mirror, or an InP/InGaAsP DBR.

[0016] According to another aspect of the present invention, a bottom AlGaInAs/AlInAs DBR mirror, an AlPSb/GaPsb DBR mirror, or an InP/InGaAsP DBR mirror is grown on an n-doped InP substrate. Then, an n-doped bottom InP spacer is grown on the bottom mirror. Beneficially, an active region having a plurality of quantum wells is then grown on the n-doped bottom InP spacer, followed by a reversed biased N++/P++ tunnel junction over the active region. An n-doped top InP spacer is beneficially grown on the tunnel junction. Also beneficially, an n-doped GaAs/Al(Ga)As top DBR is grown on the n-doped top InP spacer.

[0017] Preferably, the GaAs/Al(Ga)As top DBR is grown by a multi-step process using MOCVD. First, the growth temperature is set to 400-450 °C. Then, a 20-40 nanometer thick low temperature GaAs layer is grown on the n-doped top InP

spacer. After that, the temperature is increased to around 600 °C. A high temperature GaAs seed layer, about 100 nm thick, is then grown on the low temperature GaAs layer. Then, an insulation layer comprised of SiO_2 or Si_2N_4 is formed on the GaAs seed layer. That insulation layer is then patterned to form an opening. A high temperature GaAs layer is then grown on the GaAs seed layer. Then, a GaAs/Al(Ga)As top DBR is grown on the high temperature GaAs layer. The GaAs layer and the GaAs/Al(Ga)As mirror are beneficially grown using lateral epitaxial overgrowth.

[0018] Additional features and advantages of the invention will be set forth in the description that follows, and in part will be apparent from that description, or may be learned by practice of the invention.

BRIEF DESCRIPTION OF THE DRAWING

[0019] The accompanying drawings, which are included to provide a further understanding of the invention and which are incorporated in and constitute a part of this specification, illustrate embodiments of the invention and together with the description serve to explain the principles of the invention.

[0020] In the drawings:

[0021] Figure 1 illustrates a typical vertical cavity surface emitting laser;

[0022] Figure 2 illustrates a first embodiment vertical cavity surface emitting laser that is in accord with the principles of the present invention;

[0023] Figure 3 illustrates an intermediate structure during fabrication of the vertical cavity surface emitting laser illustrated in Figure 2;

[0024] Figure 4 illustrates another intermediate structure during fabrication of the vertical cavity surface emitting laser illustrated in Figure 2; and

[0025] Figure 5 illustrates yet another intermediate structure during fabrication of the vertical cavity surface emitting laser illustrated in Figure 2.

[0026] Note that in the drawings that like numbers designate like elements. Additionally, for explanatory convenience the descriptions use directional signals such as up and down, top and bottom, and lower and upper. Such signals, which are derived from the relative positions of the elements illustrated in the drawings, are meant to aid the understanding of the present invention, not to limit it.

DETAILED DESCRIPTION OF THE ILLUSTRATED EMBODIMENTS

[0027] The principles of the present invention are incorporated in an illustrated embodiment VCSEL having a top DBR mirror comprised of GaAs/Al(Ga)As that is grown on an InP layer. An example of such a VCSEL is the VCSEL 100 illustrated in Figure 2.

[0028] As shown in Figure 2, the VCSEL 100 includes an n-doped InP substrate 112 having an n-type electrical contact (which is not shown for clarity). Over the InP substrate 112 is an n-doped lower mirror stack 116 (a DBR) comprised of a plurality of alternating layers of materials that are suitably matched to the InP substrate. For example, the lower mirror stack 116 can be comprised of AlGaInAs/AlInAs, AlPSb/GaPsb, or InP/InGaAsP. Over the lower mirror stack 116 is an n-doped bottom InP spacer 118. The lower mirror stack 116 is beneficially grown on the InP substrate using MOCVD. Then, the bottom InP spacer 118 is grown, also

using MOCVD. An active region 120 comprised of P-N junction structures and a large number of quantum wells is then formed over the bottom InP spacer 118. The composition of the active region 120 is beneficially InP.

[0029] Over the active region 120 is a tunnel junction 122 comprised of a reverse biased n++/p++ junction. Beneficially, the tunnel junction includes a p-layer comprised of MOCVD-grown $GaAs_{(1-x)}Sb_x$. During MOVCD, TMGa (or TEGa), TMSb, and AsH_3 (or TBAs) are beneficially used to produce the $GaAs_{(1-x)}Sb_x$ layer. Beneficially, that layer's solid composition is controlled by controlling the ratio of As to Sb. The MOCVD growth temperature is between 500 °C and 650 °C. Doping is beneficially performed using CCl_4 or CBr_4 such that the resulting p-doping is greater $1x10^{19}$ cm^{-3}. In practice, a p-doping greater than $5x10^{19}$ cm^{-3} is beneficial. It should be noted that the $GaAs_{(1-x)}Sb_x$ layer can have a doping as high as $1x10^{20}$ cm^{-3} without annealing. By setting x=0.5 a tunnel junction that is lattice matched to InP is produced (but $GaAs_{(.5)}Sb_{.5}$ has a bandgap of 0.71 eV at 300K). An alternative is to set x=0.4, 0.3, or 0.23, which produce $GaAs_{(1-x)}Sb_x$ layers with bandgaps of 0.8 eV, 0.91 eV, or 1eV, but which are not lattice matched to the InP active region 120. At x= 0.3, or 0.23 the strains respectively become 1.4% or 1.95%, which, while not ideal, are much better than the 3.55% strain of AlAs on InP.

[0030] The tunnel junction 122 further includes an n-doped layer of InP, AlInAs, or of a lower bandgap material such as AlInGaAs or InGaAsP. The n-doped layer should also be heavily doped (greater than $5x10^{19}$ cm^{-3}) and very thin (less than about 10 nanometers). For good lattice matching, the VCSEL 100 uses an InP n-type layer in the tunnel junction 122.

[0031] Over the tunnel junction 122 is an n-type InP top spacer 124. Then, a top mirror structure (which includes another DBR) is disposed over the top spacer 124.

[0032] The top mirror structure is beneficially comprised of a low temperature grown GaAs buffer layer 126 over the top spacer 124, a high temperature GaAs buffer layer 128 (which acts as a seed layer) over the GaAs buffer layer 126, an insulating structure (beneficially comprised of SiO_2) 130 over most of the GaAs buffer layer 128, and a GaAs/Al(Ga)As mirror stack 132 over the insulating structure 130. A shown, the insulating structure includes an opening 131 that enables current flow through the VCSEL 100.

[0033] The top mirror structure implements a device quality GaAs/Al(Ga)As mirror stack 132 over the top spacer 124. This is beneficial because in many applications, GaAs/Al(Ga)As is considered to be the best material for Bragg mirrors because of its high refractive index contrast (GaAs:AlAs=3.377:2.893), high thermal conductivity (GaAs:AlAs=0.46:0.8), and its oxidation potential. However, GaAs/Al(Ga)As is seriously lattice mismatched with InP. Thus, to produce a device-quality GaAs/Al(Ga)As mirror stack, MOCVD is used in a multi-step process to form intermediate GaAs buffer layers.

[0034] Figure 3 illustrates the first step of the two-step process. A low temperature GaAs buffer layer 126 is formed over the InP spacer 124. The low temperature GaAs buffer layer 126 is produced by adjusting the MOCVD growth temperature to about 400-450 °C, and then MOCVD growing the low temperature GaAs buffer layer 126 to a thickness of about 20-40nm.

[0035] Referring now to Figure 4, after the low temperature GaAs buffer layer 126 is formed, the temperature is increased to around 600 °C. Then, the high temperature GaAs buffer layer 128 is grown. The GaAs buffer layer 128 acts as a seed layer for subsequent growth.

[0036] Referring now to Figure 5, after the GaAs buffer layer 128 is grown, a dielectric layer of SiO_2 (alternatively of Si_3N_4) is deposited and patterned to form the insulating structure 130. To do so, the intermediate structure shown in Figure 4 is removed from the MOCVD reactor vessel. Then, a dielectric layer of SiO_2 (alternatively Si_3N_4) is deposited on the insulating structure 130. Then, the deposited dielectric layer is patterned to produce the insulating structure 130 having the opening 131. The insulating structure 130 provides a suitable surface for lateral epitaxial overgrowth. After the insulating structure 130 formed, the intermediate structure of Figure 5 is inserted into the MOCVD reactor vessel. Referring once again to Figure 2, the GaAs/Al(Ga)As mirror stack 132 is then grown by MOCVD. That mirror stack is produced by lateral epitaxial overgrowth from the GaAs buffer layer 128 through the opening 131. The result is a high-quality mirror stack 132 having current confinement.

[0037] With the mirror stack 132 formed, an n-type conduction layer (similar to the p-type conduction layer 9 of Figure 1), an n-type GaAs cap layer (similar to the p-type GaAs cap layer 8 of Figure 1), and an n-type electrical contact (similar to the p-type electrical contact 26 of Figure 1) are produced.

[0038] The VCSEL 100 has significant advantages over prior art long wavelength InP-based VCSELs. First, the multi-step MOCVD process of forming a

low temperature GaAs layer and a high temperature GaAs seed layer enables a device quality GaAs/Al(Ga)As top mirror to be used with an AlInGaAs or InGaAsP active region 120 and an InP top spacer 124. Another advantage is that the tunnel junction 122 enables n-doped top layers to be used, which reduces optical absorption (which can be critically important in long wavelength VCSELs). Yet another advantage is the use of different DBR materials in the bottom DBR and in the top DBR. This enables maximizing the benefits of different material systems. Still another advantage is the incorporation of current confinement structures and the use of lateral epitaxial overgrowth to produce the top DBR mirror. The overall result can be VCSELs having improved performance, increased reliability, faster fabrication, and reduced cost.

[0039] It will be apparent to those skilled in the art that various modifications and variation can be made in the present invention without departing from the spirit or scope of the invention. Thus, it is intended that the present invention cover the modifications and variations of this invention provided they come within the scope of the appended claims and their equivalents.